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GALILEO PAYLOAD 10.23 MHZ MASTER CLOCK GENERATION WITH A CLOCK MONITORING AND CONTROL UNIT (CMCU)

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Abstract – **The system concept of the Galileo navigation satellite payload requires a Clock Monitoring and Control Unit (CMCU) to provide a Master Timing Reference for the generation of the navigation signal. This frequency is synthesized from one of four atomic clocks, selected by the CMCU to provide a 10 MHz reference. High requirements have to be applied to the frequency synthesizers not to degrade the frequency stability of the atomic clocks and to provide high spectral purity by acting as a clean-up circuit. As the atomic clocks are free running, their frequency offsets have to be corrected by the synthesizer in frequency steps of less than 1e-13 referred to the CMCU output. To solve these requirements, a hybrid synthesizer architecture is presented, consisting of a phase locked loop in conjunction with a DDS to generate an auxiliary frequency that is tuneable with the required fine granularity. Due to the spurious problems with conventional DDS circuits or fractional frequency dividers new noise shaping technologies are applied to shift the spurious energy to higher Fourier frequencies that are filtered out later by the PLL loop bandwidth. Furthermore to optimise the synthesizer performance with respect to Allan deviation and phase noise, the reference source and OCXO behavior have to be taken into account for the design of the loop filter.**
In this paper, the concept for the frequency synthesizer will be discussed including the higher order noise shaping applied to the generation of the auxiliary frequency and the loop filter design considerations completed by experimental results obtained with the breadboard circuit.
Keywords **– Frequency Synthesis, Galileo, CMCU**

I. INTRODUCTION

As shown in figure 1 the payload of the Galileo navigation satellite consists of a clock ensemble with two Passive H-Masers (PHM) and two Rubidium Atomic Frequency Sources (RAFS) that provide the time reference for the generation of the navigation signal. The atomic reference is selected and converted to the Master Timing Reference of 10.23 MHz by the Clock Monitoring and Control Unit (CMCU). The MTR provides the reference for the Frequency Generation and Up-conversion Unit (FGUU) to generate the master clock for the Navigation Signal Generation Unit (NSGU) and up-convert the navigation signals to their transmission frequencies. These signals pass the power amplifiers and are transmitted afterwards.
The MTR itself is synthesized in the CMCU on the basis of the four Atomic Frequency Standards (AFS) as depicted in figure 2. One active frequency synthesizer and one identical unit in hot redundancy can select independently one out of the four signal inputs fed by the 10 MHz atomic clock reference signals for the master clock generation.

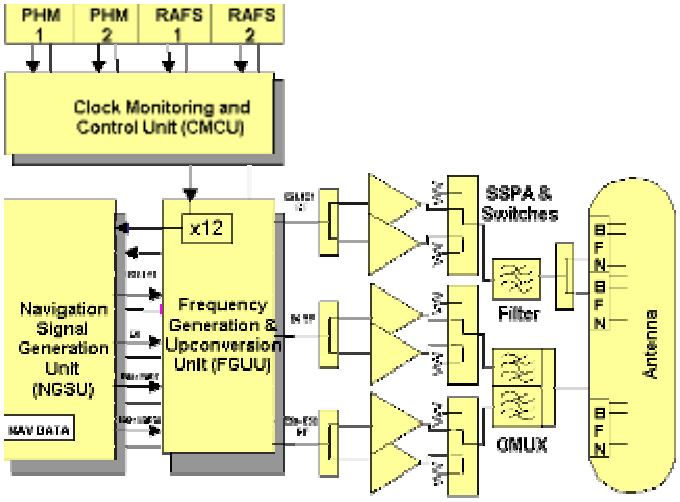

Fig. 1. Payload of the Galileo Navigation Satellite.

The output switch selects the active synthesizer and its signal is distributed to up to four identical outputs. A phase meter monitors the phase difference between the active and the hot redundant synthesizer to provide a basis for modeling the redundant clock behavior compared to the active one. The active clock can be monitored directly by observing the transmitted navigation signal.

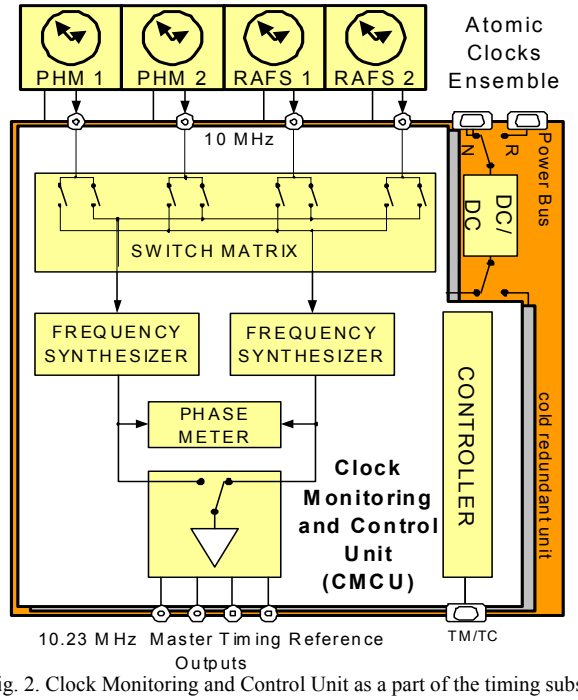

Fig. 2. Clock Monitoring and Control Unit as a part of the timing subsystem.

To increase the operational safety, a second CMCU unit is kept in cold redundancy. Furthermore it abandons a micro controller use. The TM/TC interface is implemented as hard wired logic and can be addressed by serial and high level commands. Nevertheless according to the customer needs optional features like phase synchronous output switching between active and redundant synthesizer, parameter based clock drift compensation or synthesizer adaptation to source characteristics can be implemented.

II. Concept for Frequency Synthesis

To keep the AFS untouched, their frequency offsets and drifts have to be corrected by the frequency synthesizer. Therefore the synthesizer requires a very high resolution in frequency steps of 1e-13 referred to the output frequency within an adjustment range of 1e-9. Furthermore to gain additional safety in system the CMCU is designed to act as a clean-up circuit that provides high spectral purity. To fulfill these requirements, a hybrid PLL architecture was chosen as depicted in figure 3. It consists of a DDS providing an auxiliary frequency for phase comparison into an analogue PLL.

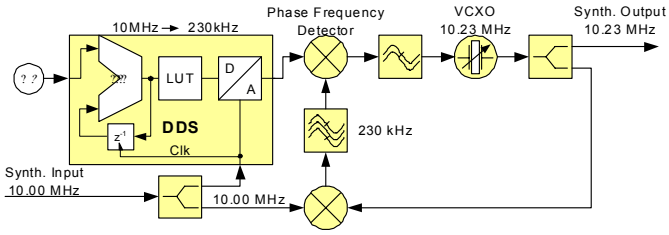

Fig. 3. CMCU synthesizer architecture.

The advantages of this concept are that the DDS can provide the 230 kHz with a high resolution in frequency step size, determined only by the bit width of the accumulator to maintain the required resolution of the synthesizer. Outside the PLL loop bandwidth, the phase noise is only determined by the VCXO properties. To take advantage of this effect that leads to improvements in phase noise and clean-up of spurs from the reference, a high-performance OCXO was chosen and the PLL response adapted to the source characteristics. Furthermore temperature and aging dependent phase drifts are corrected by the PLL, that could otherwise degrade the Allan deviation.

III. Reduction of DDS Spurs by Noise Shaping

The main drawback of the concept is the DDS generating spurious due to phase truncation, amplitude truncation and the non-linearity of the DAC as described in [1]. Efforts have to be done to minimize these spurs inside the PLL loop bandwidth. First approaches to alleviate the spurs due to phase truncation were presented in [2,3] by alternating the lowest bit of the accumulator with each clock cycle. Other approaches are based on adding noise at various points of the loop [4 ,6]. These approaches randomize the truncation errors without taking them into account. In [5] a idea is presented based on first order noise shaping, applied only to the phase truncation error. Our approach to solve this problem is to take these truncation errors as inputs for two higher order noise shapers as shown in figure 4.

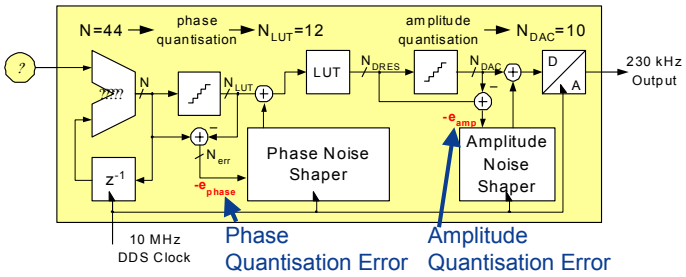

Fig. 4. Insertion of noise shapers into the DDS architecture.

In this case the energy of the errors is randomized and by differentiating it in the noise shaper. It is shifted up to higher frequencies away from the used frequency range. Figure 5 depicts simulated results for a set-up as shown in figure 4 consisting of a 44 bit phase accumulator truncated to the 12 most significant bits for the look-up table and 10 bits of DAC resolution.

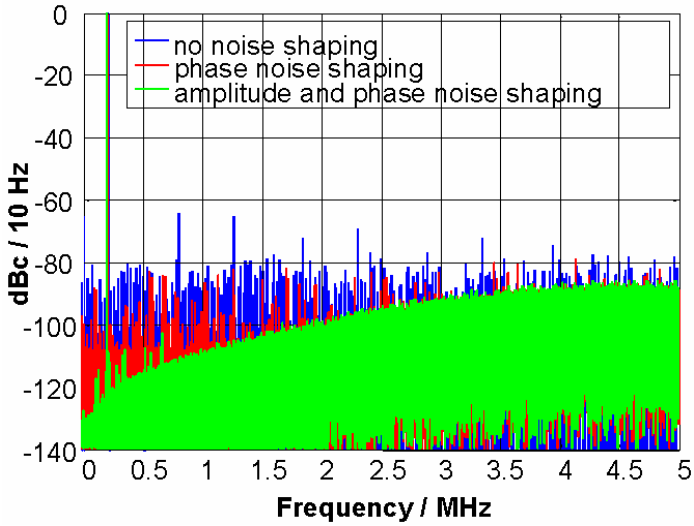

Fig. 5. Simulated output spectra of the DDS with improvements by amplitude and phase noise shaping.

The blue curve shows the simulated output spectrum of the DDS without any noise shaping. The worst case spurs are determined in [2] to be less than -60 dBc. By applying the truncated accumulator bits to a noise shaper and adding its output to the LUT input, first reductions can be achieved as given by the red curve. If in addition the amplitude quantization errors are noise shaped and added to the DAC input signal in a similar way, significant reductions can be obtained in the low frequency range.

An experimental verification of the simulation is depicted in figure 6. The blue curve shows the DDS output spectrum without noise shaping and the red curve with noise shaping of the amplitude and phase truncation errors.

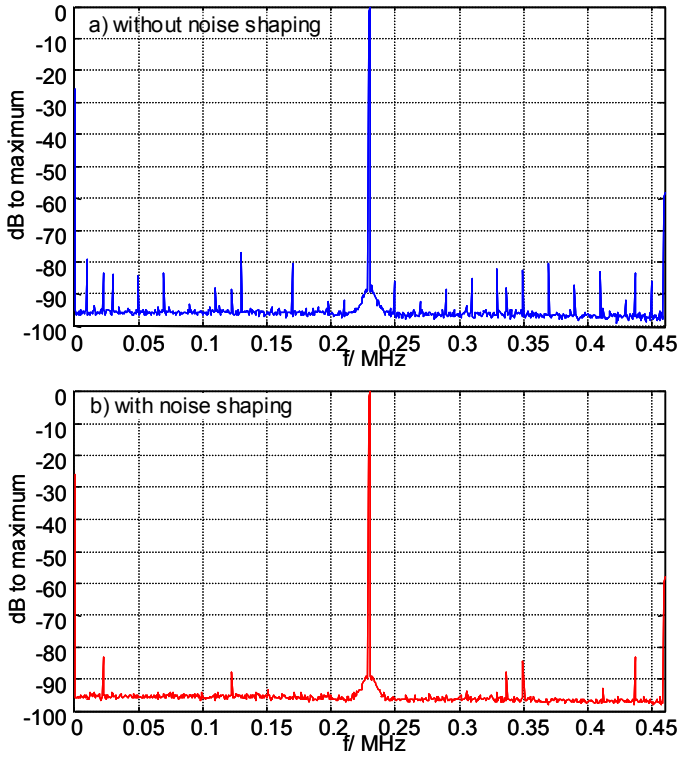

Fig. 6. Measured output spectra of the DDS with and without noise shaping (spectrum analyzer resolution bandwidth 10 Hz).

Despite a significant reduction of spurious, no compete removal could be achieved, mainly due to non-linearities of the DAC and its switching distortions.

V. Adaptation of the PLL to the Atomic References

In order to provide an optimum design with high spectral purity for clean-up, the PLL loop bandwidth has to be chosen as small as possible. On the other hand side the preservation of the long term stability of the reference demands a large loop bandwidth for a fast compensation of the VCXO drifts. The trade-off between this two requirements leads to the selection of a double-ovenized OCXO with a 3rd overtone SC-cut crystal, that provides high spectral purity as well as sufficient short term stability. Figure 7 and 8 show the simulations for the PLL behavior in the time and frequency domain based on the specifications of the used OCXO and the PHM as a reference source as well as other noise sources located within the PLL not shown in the diagram. The PLL loop response was adjusted in that way to follow the ADEV of the reference source for times larger than one second to fulfill the given specifications for the Galileo Signal Test Bed (GSTB). This leads to a loop corner frequency of approximately 0.2 Hz and reference noise suppression for higher Fourier frequencies according to the closed loop transfer function of the PLL.

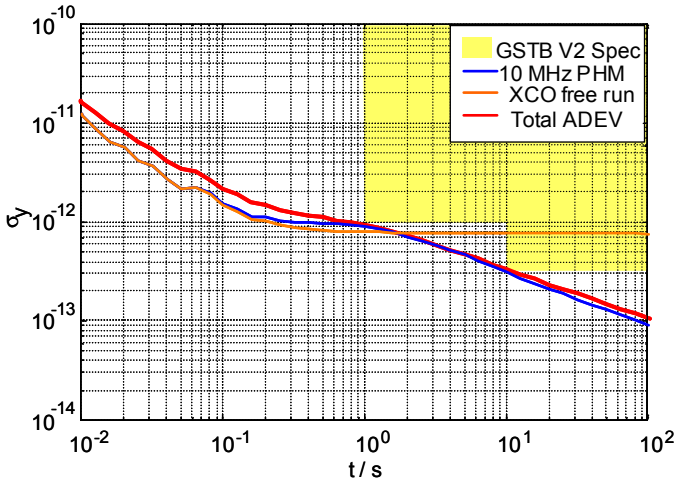

Fig. 7. Simulated Allan Deviation PLL based on the free running OCXO behavior and the reference source.

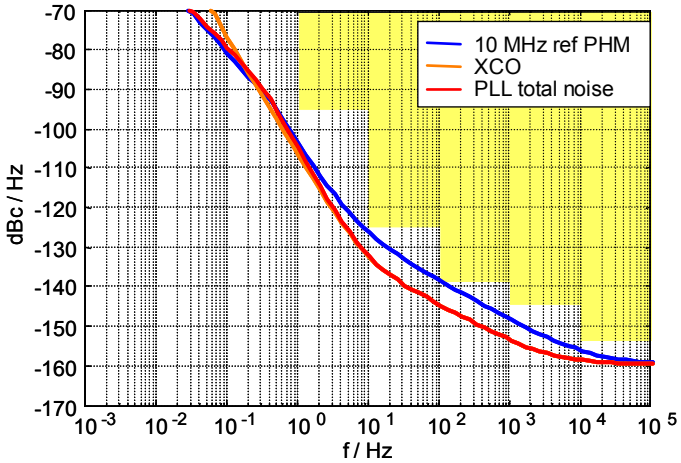

Fig. 8. Simulated single sideband phase noise for the PLL based on the free running OCXO behavior and the reference source.

VI. Measurement Results

First measurement results obtained with a breadboard circuit are depicted in figure 9 and 10. The reference for both measurements was a high performance 10 MHz OCXO with an ADEV below 7e-13 for time intervals of 1 to 100 seconds. The phase noise was measured against the same type of OCXO as used in the synthesizer but without any corrections for its noise contributions so that the measurement reflects a more pessimistic view. For the measurement of the ADEV introduced by the synthesizer, its input was measured against its output with a time and frequency analyzer. The curve shows the change in slope at the PLL loop time constant of 5 seconds from $1/\sqrt{f}$ where the reference and the OCXO contribute individually to $1/f$ for larger intervals where deviations are corrected by the PLL. The yellow mask reflects the GSTB requirements.

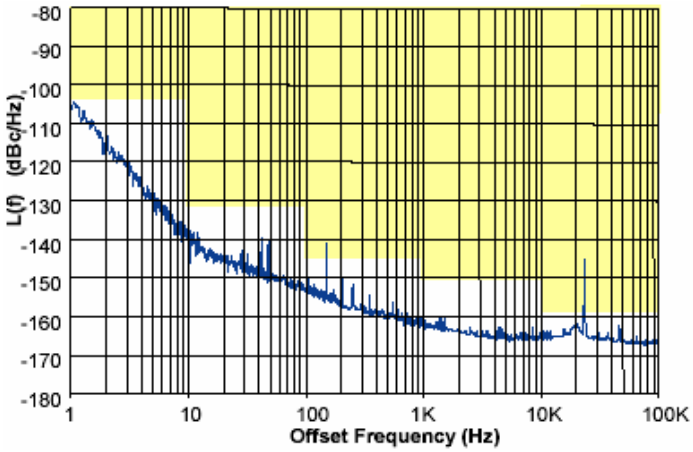

Fig. 9. Single sideband phase noise curve of the whole synthesizer.

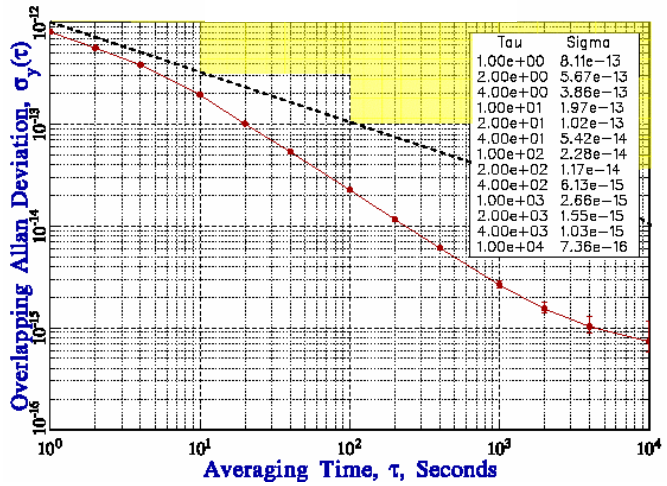

Fig. 10. Allan deviation of the synthesizer comparing input and output frequency.

IV. Conclusion

In this contribution a frequency synthesizer design for the Clock Monitoring and Control Unit of the Galileo navigation satellite payload was presented converting the 10 MHz atomic reference to the Master Time Reference 10.23 MHz. To fulfill the demanding requirements for phase noise and Allan deviation while providing a high resolution in frequency step size of the output frequency, a hybrid PLL was chosen consisting of a DDS providing the fine granularity in combination with a conventional analogue PLL. To overcome the spurious disadvantages of the DDS, a new noise shaping method was presented. It incorporates the errors due to amplitude and phase truncation within the DDS by randomizing their energy in the frequency domain and shifting them away from the used bandwidth towards the Nyquist frequency. Simulative and experimental results were shown to demonstrate the advantages of this method.

Furthermore the design of the PLL was discussed with respect to its corner frequency adapted to the reference sources and its OCXO to provide highest spectral purity while not degrading the Allan deviation of the reference source for time intervals of 1 second and above. The paper concluded with experimental results demonstrating the feasibility of the prior simulative results.

Acknowledgment

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